CLAIMS

What is claimed is:

1. A circuit comprising:

a delay chain, which is capable of receiving an input signal and producing multiple delayed signals that represent delayed versions of the input signal, wherein the multiple delayed signals are separated by a first phase increment;

multiple interpolator blocks, operably coupled to the delay chain, wherein consecutive ones of the multiple interpolator blocks are capable of receiving and interpolating between consecutive ones of the multiple delayed signals to produce an interpolated version of the input signal, wherein the interpolated version is delayed to one of multiple, intermediate delay values that are separated by a second phase increment that is smaller than the first phase increment; and

a current source select signal generator circuit, operably coupled to the multiple interpolator blocks, which includes a split current source, and which is capable of providing variable current source select signals to the multiple interpolator blocks to control interpolation between the consecutive ones of the multiple delayed signals.

2. The circuit of claim 1, wherein each of the multiple interpolator blocks comprises:

an interpolator block current source having a first number of transistor legs, which are selectively activatable based on a value of an input bias signal to the current source; and

wherein the split current source of the current source select signal generator circuit comprises:

a first current source having a second number of transistor legs that is a first fraction of the first number; and

a second current source having a third number of transistor legs that is a second fraction of the first number.

3. The circuit of claim 2, wherein the first fraction and the second fraction are ½.

4. The circuit of claim 1, further comprising:

a differential comparator, operably coupled to the multiple interpolator blocks, which is capable of producing, as an output, the interpolated version of the input signal based on signals received from the multiple interpolator blocks.

5. The circuit of claim 1, wherein the first phase increment is approximately equal to:

$$(1/F_{MAX}) / N,$$

wherein F_{MAX} equals a maximum frequency of the input signal, and N equals a number of delay chain stages.

6. The circuit of claim 1, wherein the second phase increment is approximately equal to:

$$(1/F_{MAX}) / (N*M),$$

wherein F_{MAX} equals a maximum frequency of the input signal, N equals a number of delay chain stages, and M equals a number of intermediate phase delays.

7. A circuit comprising:

multiple interpolator blocks, wherein consecutive ones of the multiple interpolator blocks are used to interpolate between a first multi-phase signal and a second multi-phase signal that are separated by a first phase increment, and wherein each interpolator block includes

an interpolator block current source having a first number of transistor legs, wherein a number of activated legs, at any given time, is based on a variable current source select signal, and

multiple input signal gates, which are activatable in response to a multi-phase signal; and

a current source select signal generator circuit, operably coupled to the multiple interpolator blocks, and which is capable of providing variable current source select signals to the consecutive ones of the multiple interpolator blocks, and wherein the current source select signal generator circuit includes a split current source.

8. The circuit of claim 7, wherein the split current source of the current source select signal generator circuit comprises:

a first current source having a second number of transistor legs that equals a first fraction of the first number; and

a second current source having a third number of transistor legs that equals a second fraction of the first number.

9. The circuit of claim 7, wherein the first phase increment is approximately equal to:

$$(1/F_{MAX}) / N,$$

wherein F_{MAX} equals a maximum frequency of the input signal, and N equals a number of delay chain stages.

10. The circuit of claim 7, wherein the first multi-phase signal and the second multi-phase signal represent delayed versions of an input signal, and wherein the circuit produces an interpolated version of the input signal, and wherein the interpolated version is delayed to one of multiple, intermediate delay values that are separated by a second phase increment that is smaller than the first phase increment.

11. The circuit of claim 10, wherein the second phase increment is approximately equal to:

$$(1/F_{MAX}) / (N*M),$$

wherein F_{MAX} equals a maximum frequency of the input signal, N equals a number of delay chain stages, and M equals the first number of transistor legs.

12. An integrated circuit comprising:

a delay chain, which is capable of receiving an input signal and producing multiple delayed signals that represent delayed versions of the input signal, wherein the multiple delayed signals are separated by a first phase increment;

multiple interpolator blocks, operably coupled to the delay chain, wherein consecutive ones of the multiple interpolator blocks are capable of receiving and interpolating between consecutive ones of the multiple delayed signals to produce an interpolated version of the input signal, wherein the interpolated version is delayed to one of multiple, intermediate delay values that are separated by a second phase increment that is smaller than the first phase increment; and

a current source select signal generator circuit, operably coupled to the multiple interpolator blocks, which includes a split current source, and which is capable of providing variable current source select signals to the multiple interpolator blocks to control interpolation between the consecutive ones of the multiple delayed signals.

13. The integrated circuit of claim 12, wherein each of the multiple interpolator blocks comprises:

an interpolator block current source having a first number of transistor legs, which are selectively activatable based on a value of an input bias signal to the current source; and

wherein the split current source of the current source select signal generator circuit comprises:

a first current source having a second number of transistor legs that is a first fraction of the first number; and

a second current source having a third number of transistor legs that is a second fraction of the first number.

14. The integrated circuit of claim 12, further comprising:

logic circuitry, which is capable of producing a delay value signal, wherein the delay value signal indicates which two blocks of the multiple interpolator blocks are to be used as the consecutive interpolator blocks from which the interpolated version of the input signal is produced.

15. A system comprising:

at least one integrated circuit, which includes a variable-delay signal generator circuit, wherein the variable-delay signal generator circuit includes

a delay chain, which is capable of receiving an input signal and producing multiple delayed signals that represent delayed versions of the input signal, wherein the multiple delayed signals are separated by a first phase increment;

multiple interpolator blocks, operably coupled to the delay chain, wherein consecutive ones of the multiple interpolator blocks are capable of receiving and interpolating between consecutive ones of the multiple delayed signals to produce an interpolated version of the input signal, wherein the interpolated version is delayed to one of multiple, intermediate delay values that are separated by a second phase increment that is smaller than the first phase increment; and

a current source select signal generator circuit, operably coupled to the multiple interpolator blocks, which includes a split current source, and which is capable of providing variable current source select signals to the multiple interpolator blocks to control interpolation between the consecutive ones of the multiple delayed signals.

16. The system of claim 15, wherein each of the multiple interpolator blocks comprises:

an interpolator block current source having a first number of transistor legs, which are selectively activatable based on a value of an input bias signal to the current source; and

wherein the split current source of the current source select signal generator circuit comprises:

a first current source having a second number of transistor legs that is a first fraction of the first number; and

a second current source having a third number of transistor legs that is a second fraction of the first number.

17. The system of claim 15, further comprising:

a network interface to couple to one or more networks.

18. The system of claim 15, further comprising:

a wireless medium interface to couple to one or more external wireless systems.

19. The system of claim 15, further comprising:

a battery interface, which is capable of receiving one or more batteries, which can provide power to various electronic components of the system.

20. A test assembly comprising:

an integrated circuit, which includes a variable-delay signal generator circuit that includes

a delay chain, which is capable of receiving an input signal and producing multiple delayed signals that represent delayed versions of the input signal, wherein the multiple delayed signals are separated by a first phase increment;

multiple interpolator blocks, operably coupled to the delay chain, wherein consecutive ones of the multiple interpolator blocks are capable of receiving and interpolating between consecutive ones of the multiple delayed signals to produce an interpolated version of the input signal, wherein the interpolated version is delayed to one of multiple, intermediate delay values that are separated by a second phase increment that is smaller than the first phase increment; and

a current source select signal generator circuit, operably coupled to the multiple interpolator blocks, which includes a split current source, and which is capable of providing variable current source select signals to the multiple interpolator blocks to control interpolation between the consecutive ones of the multiple delayed signals.

21. The test assembly of claim 20, wherein each of the multiple interpolator blocks comprises:

an interpolator block current source having a first number of transistor legs, which are selectively activatable based on a value of an input bias signal to the current source; and

wherein the split current source of the current source select signal generator circuit comprises:

a first current source having a second number of transistor legs that is a first fraction of the first number; and

a second current source having a third number of transistor legs that is a second fraction of the first number.

22. The test assembly of claim 20, wherein the integrated circuit further comprises:

logic circuitry, which is capable of producing a delay value signal, wherein the delay value signal indicates which two blocks of the multiple interpolator blocks are to be used as the consecutive interpolator blocks from which the interpolated version of the input signal is produced.

23. A method comprising:

generating current source select signals using a split current source;

receiving, by two consecutive interpolator blocks, two consecutive multi-phase signals, wherein the two consecutive multi-phase signals are separated by a first phase increment; and

interpolating between the two consecutive multi-phase signals by varying a first current produced by a first block of the consecutive interpolator blocks, and a second current produced by a second block of the consecutive interpolator blocks, wherein the first current and the second current have values that depend on the current source select signals, and wherein the combination of the first current and the second current results in an interpolator output signal that is delayed to one of multiple intermediate phase delay values.

24. The method of claim 23, further comprising:

producing, by a delay chain, the two consecutive multi-phase signals.

25. The method of claim 23, wherein interpolating comprises:

turning on a first number of transistor legs of a first current source of the first block, resulting in the first current, wherein the first number depends on a first current source select signal; and

turning on a second number of transistor legs of a second current source of the second block, resulting in the second current, wherein the second number depends on a second current source select signal.